NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. M4065.0112/P112-A

Total pages in this submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

MICROLENS ARRAY WITH IMPROVED FILL FACTOR

and invented by:

Howard E. Rhodes

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

[ ] Continuation [X] Divisional

[ ] Continuation-in-part (CIP) of prior application No.: 09/357,168

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 28 pages(s) and including the following:
   a. [X] Descriptive title of the invention
   b. [ ] Cross references to related applications *(if applicable)*
   c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   d. [ ] Reference to microfiche appendix *(if applicable)*
   e. [X] Background of the invention
   f. [X] Brief summary of the invention
   g. [X] Brief description of the drawings *(if drawings filed)*
   h. [X] Detailed description
   i. [X] Claims as classified below
   j. [X] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [ ] Formal [X] Informal Number of sheets: 5

4. [X] Oath or Declaration

   a. [ ] Newly executed (original or copy) [ ] Unexecuted

   b. [X] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [X] Without Power of Attorney

5. [X] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [ ] Assignment papers *(cover sheet & document(s))*

9. [X] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [X] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS citations

12. [X] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	40	- 20 =	20	x $18.00	$360.00
Independent Claims	4	- 3 =	1	x $80.00	$80.00
Multiple Dependent Claims (check if applicable)		☐			
Other Fees (specify purpose):					
				BASIC FEE	$710.00
				TOTAL FILING FEE	$1,150.00

☒ A check in the amount of $1,150.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of _____ as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

Dated: October 12, 2000

Mark J. Thronson
Attorney Reg. No.: 33,082
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

PATENT
Docket No.: M4065.0112/P112-A
Micron Ref.: 98-0121-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Howard E. Rhodes

Serial No.: Not Yet Assigned
Divisional of Serial No. 09/357,168

Group Art Unit: Not Yet Assigned

Filed: October 12, 2000

Examiner: Not Yet Assigned

For: MICROLENS ARRAY WITH IMPROVED FILL FACTOR

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

Preliminary to examination, please amend the above-referenced application as follows:

IN THE SPECIFICATION:

Page 1, after the title, insert the following sentence: --This is a divisional of U.S. Patent Application No. 09/357,168, filed July 19, 1999, the entire disclosure of which is incorporated herein by reference.---.

IN THE CLAIMS:

Cancel claims 1-59, without prejudice.

REMARKS

Claims 60-99 remain in the application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications. Allowance of the application is solicited.

Dated: October 12, 2000

Respectfully submitted,

By _____

Mark J. Thronson
Registration No.: 33,082
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

Attorneys for Applicant

Docket No.: M4065.0112/P112
Micron Ref.: 98-0121.00/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT

Title:

MICROLENS ARRAY WITH IMPROVED FILL FACTOR

Inventor:

Howard E. Rhodes

Dickstein, Shapiro, Morin &
Oshinsky LLP
Suite 400
2101 L Street, N.W.
Washington, D.C. 20037
(202) 785-9700

MICROLENS ARRAY WITH IMPROVED FILL FACTOR

FIELD OF THE INVENTION

The present invention relates generally to a microlens array for use in a solid-state image sensor and in particular to a microlens array having an improved fill factor, and a method for producing the same.

BACKGROUND OF THE INVENTION

Solid-state image sensors, also known as imagers, were developed in the late 1960s and early 1970s primarily for television image acquisition, transmission, and display. An imager absorbs incident radiation of a particular wavelength (such as optical photons, x-rays, or the like) and generates an electrical signal corresponding to the absorbed radiation. There are a number of different types of semiconductor-based imagers, including charge coupled devices (CCDs), photodiode arrays, charge injection devices (CIDs), hybrid focal plan arrays, and CMOS imagers. Current applications of solid-state imagers include cameras, scanners, machine vision systems, vehicle navigation systems, video telephones, computer input devices, surveillance systems, auto focus systems, star trackers, motion detector systems, image stabilization systems and data compression systems for high-definition television.

These imagers typically consist of an array of pixel cells containing photosensors, where each pixel produces a signal corresponding to the intensity of light impinging on that element when an image is focused on the array. These signals may then be used, for example, to display a corresponding image on a monitor or otherwise used to provide information about the optical image. The photosensors are typically phototransistors, photoconductors or photodiodes, where the conductivity of the photosensor or the charge stored in a diffusion corresponds to the intensity of light impinging on the photosensor. The

magnitude of the signal produced by each pixel, therefore, is proportional to the amount of light impinging on the photosensor.

It is known in the art to use a microlens array with an imager array, wherein the microlens array comprises a convex microlens for each pixel. The microlenses refract incident radiation from the circuitry region of the pixel to the photosensor region, thereby increasing the amount of light reaching the photosensor and thereby increasing the fill factor of the pixels. Other uses of microlens arrays include intensifying illuminating light on the pixels of a nonluminescent display device such as a liquid crystal display device to increase the brightness of the display, forming an image to be printed in a liquid crystal or light emitting diode printer, and as focusing means for coupling a luminescent device or a receptive device to an optical fiber.

Despite the use of microlens arrays, a large amount of light incident on an imager is not directed onto the photosensor due to the geometry of the microlens array. In particular, light incident on the space between individual lenses (the lens-lens space), and on the edges of the pixel beyond the edges of an individual lens remains uncaptured by the microlens, and never impacts the photosensor. Additionally, the typical practice of forming the microlens array on a separate substrate from the pixel array leads to problems of lens-pixel alignment that results in additional lost light.

There is needed, therefore, a microlens array having an improved fill factor formed on the same substrate as a pixel array. A simple method of fabricating a microlens array having an improved fill factor is also needed.

SUMMARY OF THE INVENTION

The present invention provides a microlens array for use in a solid-state imager having a pixel array, wherein each microlens of the microlens array may correspond to a pixel cell of the imager pixel array. Each microlens consists of two layers: a lower refractive layer, and an upper insulation layer. The refractive layer is formed of transparent material with a suitable refractive index, which may be an optical thermoplastic such as polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, or polystyrene, a polyimide, a thermoset resin such as an epoxy resin, a photosensitive gelatin, or a radiation curable resin such as acrylate, methacrylate, urethane acrylate, epoxy acrylate, or polyester acrylate. The insulation layer is radiation-transparent and assists in capturing light at the edges of the pixel, thereby improving the fill factor of the microlens array. Suitable materials for the insulation layer include silicon insulators such as silicon oxide, silicon nitride, or silicon oxynitride that have been formed by a low temperature process. Also provided are methods for forming the microlens array of the present invention.

Additional advantages and features of the present invention will be apparent from the following detailed description and drawings which illustrate preferred embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a side cross-sectional view showing the principal elements of a solid-state imager having a microlens array according to one embodiment of the present invention.

Figure 2 is a top view of the microlens array of Fig. 1.

Figure 3 is a cross-sectional view of a CMOS imager pixel cell having a microlens constructed in accordance with an embodiment of the present invention.

Figure 4 is a representative diagram of the CMOS imager pixel cell of Fig. 3.

Figure 5 is a cross-sectional view of a semiconductor wafer undergoing the process of a preferred embodiment of the invention.

Figure 6 shows the wafer of Fig. 5 at a processing step subsequent to that shown in Fig. 5.

Figure 7 shows the wafer of Fig. 5 at a processing step subsequent to that shown in Fig. 6.

Figure 8 shows the wafer of Fig. 5 at a processing step subsequent to that shown in Fig. 7.

Figure 9 is an illustration of a computer system having an imager with a microlens array according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes

may be made without departing from the spirit and scope of the present invention.

The terms "wafer" and "substrate" are to be understood as including silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, germanium, or gallium arsenide. The term "pixel" refers to a picture element unit cell containing a photosensor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative CMOS imager pixel is illustrated in the figures and description herein. However, this is just one example of the type of imagers and pixel cells thereof with which the invention may be used. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Referring now to the drawings, where like elements are designated by like reference numerals, a solid-state imager 20 containing an embodiment of the microlens array 22 of the present invention is shown in Figs. 1 and 2. The imager 20 comprises a microlens array or light condensing layer 22 formed over a pixel array 26 as part of the same substrate 30, which may be any of the types of substrate described above. The pixel array 26 is comprised of a plurality of pixel sensor cells 28 formed in the substrate, and is covered by a protective layer 24 that acts as a passivation and planarization layer for the imager 20. Protective layer 24 may be a layer of BPSG, PSG, BSG, silicon dioxide, silicon nitride,

polyimide, or other well-known light transmissive insulator. The microlens array or light condensing layer 22 is formed on the protective layer 24, and is comprised of a plurality of microlenses 32. In a preferred embodiment, depicted in Figs. 1 and 2, the microlens array 22 is formed so that a microlens 32 is formed above each pixel cell 28. The microlens array 22 is formed such that the focal point of the array is centered over the photosensitive elements in each pixel cell 28. The device also includes a spacer layer 25 under the mircolens array 22. The thickness of spacer layer 25 is adjusted such that the photosensitive element is at a focal point for the light traveling through microlens array 22. The spacer layer 25 may have a thickness of from about 1 μm to about 20 μm. If desired, a color filter, fluorescent material film, or other device for converting the wavelength of incident light may be used with the pixel array 26 by placing the device on top of the protective layer 24 and beneath the microlens array 22.

As can be seen in Figs. 3 through 4, each pixel sensor cell 28 contains a photosensor 34, which may be a photodiode, photogate, or the like. A photogate photosensor 34 is depicted in Figs. 3 through 4. An applied control signal PG is applied to the photogate 34 so that when incident radiation 100 in the form of photons strikes the photosensor 34 the photo-generated electrons accumulate in the doped region 36 under the photosensor 34. A transfer transistor 38 is located next to the photosensor 34, and has source and drain regions 36, 40 and a gate stack 42 controlled by a transfer signal TX. The drain region 40 is also called a floating diffusion region or a floating diffusion node, and it passes charge received from the photosensor 34 to output transistors 44, 46 and then to readout circuitry 48. A reset transistor 50 comprised of doped regions 40, 52 and gate stack 54 is controlled by a reset signal RST which operates to reset the floating diffusion region 40 to a predetermined initial voltage just prior to signal readout.

As can best be seen in Fig. 3, the gate stacks 42, 54 of the pixel cell 28 include a silicon dioxide or silicon nitride insulator 56 on the substrate 30, which in this example is a p-type substrate, a conductive layer 58 of doped polysilicon, tungsten, or other suitable material over the insulating layer 56, and an insulating cap layer 60 of, for example, silicon dioxide, silicon nitride, or ONO (oxide-nitride-oxide). A silicide layer 59 may be used between the polysilicon layer 58 and the cap 60, if desired. Insulating sidewalls 62 are also formed on the sides of the gate stacks 42, 54. These sidewalls may be formed of, for example, silicon dioxide, silicon nitride, or ONO. A field oxide layer 64 around the pixel cell 28 serves to isolate it from other pixel cells in the array. A second gate oxide layer 57 may be grown on the silicon substrate and the photogate semi-transparent conductor 66 is patterned. In the case that the photosensor is a photodiode, no second gate oxide layer 57 and no photogate semi-transparent conductor 66 is required. Furthermore, for the case of a photodiode, a transfer gate is optional.

The microlens array 22 of a preferred embodiment is formed so that a microlens 32 is formed above each pixel cell 28, as can be seen in Figs. 3 through 5. The microlens 32 has three transparent layers, a refractive layer 70 and an insulation layer 72 and spacer layer 25. The refractive layer 70 is fashioned from transparent material with a suitable refractive index which may be an optical thermoplastic such as polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, or polystyrene, a polyimide, a thermoset resin such as an epoxy resin, a photosensitive gelatin, or a radiation curable resin such as acrylate, methacrylate, urethane acrylate, epoxy acrylate, or polyester acrylate. The insulation layer 72 is also transparent, and is made from a silicon insulator such as silicon oxide, silicon nitride, or silicon oxynitride that has been formed by a low temperature process, such as a plasma enhanced chemical vapor deposition process conducted at a temperature within the range of approximately 200 to

400 degrees Celsius. The shape of the microlens 32 as seen from above may be circular, lenticular, ovoid, rectangular, hexagonal or any other suitable shape.

The microlens 32 operates to refract incident radiation 100 from the circuitry region of the pixel cell 28 to the photosensor region. As can be seen in Fig. 3, the microlens 32 is a plano-convex lens having a generally semi-circular cross-section. Light radiation 100 is typically perpendicularly incident to the pixel cell 28, and if no microlens were used, light radiation not directed at the photosensor 34 would not ever strike it, i.e., light radiation directed at the reset gate 54, for example, would strike the reset gate 54 and not the photosensor 34. Use of a microlens, which because of its convex shape acts to condense or focus incident radiation 100 into a smaller area than that of the microlens 32, enables light radiation not originally directed at the photosensor 34 to be redirected towards the photosensor 34. For example, light radiation 100 incident on an outer edge of the microlens 32 is refracted as it passes through the microlens towards the optical axis of the microlens 32, which is positioned over the photosensor 34, and therefore strikes the photosensor 34, whereas an unrefracted beam would not strike the photosensor 34.

As pixel sensor cells 28 decrease in size due to the demand for increased array density, complications in conventional photolithography and other patterning processes result in the formation of conventional microlenses that do not completely cover the pixel sensor cell 28. This can be seen mostly clearly in Fig. 3, wherein the refractive layer 70 extends across a large portion of the pixel cell 28, but due to the limitations of the patterning process does not cover the entire pixel cell 28. The present invention provides an insulation layer 72 covering the refractive layer 70 , thereby effectively expanding the area of the pixel cell 28 that is covered by a refractive surface, so that a greater proportion of radiation incident on the pixel cell 28 is directed to the photosensor 34, thereby

improving the fill factor of the pixel sensor cell 28. The microlens array 22 can be used in a CMOS imager 20, as is shown in Figs. 1, 3 and 4, or may be used in a CCD imager.

The microlens array 22 is manufactured through a process described as follows, and illustrated by Figs. 6 through 9. Referring now to Fig. 6, a substrate 30, which may be any of the types of substrates described above, having a pixel array 26, peripheral circuits, contacts and wiring formed thereon by well-known methods, is provided. A protective layer 24 of BPSG, BSG, PSG, silicon dioxide, silicon nitride or the like is formed over the pixel array 26 to passivate it and to provide a planarized surface. A spacing layer 25 is formed over the protective layer 24. A lens forming layer 80 is formed on the spacer layer 25 by spin-coating or other suitable means. The lens forming layer 80 may be an optical thermoplastic such as polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, or polystyrene, a polyimide, a thermoset resin such as an epoxy resin, a photosensitive gelatin, or a radiation curable resin such as acrylate, methacrylate, urethane acrylate, epoxy acrylate, or polyester acrylate.

Next, as shown in Fig. 7, the lens forming layer 80 is patterned by conventional photolithography, or other suitable means, to form a plurality of lens forming regions 82. In the exemplary embodiment illustrated, each lens forming region 82 overlies a pixel cell 28, although alternative constructions in which a lens forming region 82 overlies multiple pixel cells 28 are foreseen. The shape of the lens forming regions 82 as seen from above may be circular, lenticular, ovoid, rectangular, hexagonal or any other suitable shape.

Referring now to Fig. 8, the substrate 30 is then treated, by heat treatment or other suitable treatment, to form refractive lenses 70 from the lens forming regions 82. The treatment used to form the refractive lenses 70 depends

on the material used to form the lens forming layer 80. If the material of the lens forming layer 80 may be heat treated, then heat treatment processes such as baking may be used. If the material is extremely photosensitive, then special light exposure techniques may be used, as further described below.

Heat treatment relies on the use of flowable materials such as optical thermoplastics, polyimides, and thermoset resins, which may be melted at relatively low temperatures to produce a smooth-surfaced lens. A typical baking process involves heating the substrate 30 at a temperature of approximately 100 to 350 degrees Celsius for a suitable length of time, such as 30 minutes. As a result of the heat applied, the lens forming regions 82 melt and surface tension in the resultant liquid results in the formation of a smooth convex lens 70 with a semi-circular cross-section.

Certain photosensitive materials such as gelatin and radiation curable resins exhibit a phenomenon in which, when selectively exposed to light, unreacted compounds move from the unexposed regions to the exposed regions, resulting in a swelling of the exposed regions. This phenomenon may be used to form refractive lenses 70 from the lens forming regions 82. The lens forming regions 82 are selectively illuminated with light from a mercury lamp or the like through the top or bottom of the substrate, which has been masked with a photomask or other suitable device for creating a lens pattern. The illumination time depends on the thickness of the lens forming regions 82, the degree of parallelism of the light beams, and the intensity of the light used, but should be sufficient to cause the lens forming regions 82 to swell into smooth convex lenses 70 having a generally semi-circular cross-section.

Fig. 9 shows the next step of the process, in which a transparent insulation layer 72 is formed on the lenses 70 via a low temperature deposition

process such as plasma enhanced chemical vapor deposition (CVD). The low temperatures are within the range of approximately 200 to 400 degrees Celsius. The transparent insulation layer 72 may be formed of a silicon insulator such as silicon oxide, silicon nitride, or silicon oxynitride that is transparent to radiation. A CVD process is especially preferred if the transparent insulation layer 72 is formed from silicon oxide, because the CVD process permits the use of tetraethylorthosilicate (TEOS) as the silicon source, as opposed to silane, and therefore results in improved conformal deposition.

The microlens array 22 is essentially complete at this stage, and conventional processing methods may now be performed to package the imager 20. Pixel arrays having the microlens arrays of the present invention, and described with reference to Figs. 1-9, may be further processed as known in the art to arrive at CMOS, CCD, or other imagers. If desired, the imager 20 may be combined with a processor, such as a CPU, digital signal processor or microprocessor, in a single integrated circuit, and may be used in a processor system such as the typical processor-based system illustrated generally at 400 in Fig. 10. A processor based system is exemplary of a system having digital circuits which could include CMOS or other imager devices. Without being limiting, such a system could include a computer system, camera system, scanner, machine vision system, vehicle navigation system, video telephone, surveillance system, auto focus system, star tracker system, motion detection system, image stabilization system and data compression system for high-definition television, all of which can utilize the present invention.

As shown in Fig. 10, a processor system such as a computer system, for example, generally comprises a central processing unit (CPU) 444, e.g., a microprocessor, that communicates with an input/output (I/O) device 446 over a bus 452. The imager 20 also communicates with the system over bus 452.

The computer system 400 also includes random access memory (RAM) 448, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 454 and a compact disk (CD) ROM drive 456 which also communicate with CPU 444 over the bus 452. The imager 20 is preferably constructed as an integrated circuit, with or without memory storage, which includes a microlens array 22 having an improved fill factor, as previously described with respect to Figs. 1 through 9.

As can be seen by the embodiments described herein, the present invention encompasses a microlens array for use in a solid-state imager such as a CMOS imager or CCD imager. The microlens array has an improved fill factor due to the presence of multi-layer lenses having an insulation layer over a refractive layer.

It should again be noted that although the invention has been described with specific reference to imaging circuits having a pixel array, the invention has broader applicability and may be used in any imaging apparatus. Similarly, the process described above is but one method of many that could be used. The above description and drawings illustrate preferred embodiments which achieve the objects, features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. Any modification of the present invention which comes within the spirit and scope of the following claims should be considered part of the present invention.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A microlens array for use in an imaging device comprising:

an imaging array;

a light condensing layer provided on said imaging array, said light condensing layer having a plurality of microlenses each corresponding to one or more pixels of said array; and

a transparent insulation layer formed on said light condensing layer.

2. The microlens array of claim 1, wherein said light condensing layer is a layer of optical thermoplastic.

3. The microlens array of claim 2, wherein the optical thermoplastic is selected from the group consisting of polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, and polystyrene.

4. The microlens array of claim 1, wherein said light condensing layer is a layer of polyimide.

5. The microlens array of claim 1, wherein said light condensing layer is a layer of thermoset resin.

6. The microlens array of claim 5, wherein the thermoset resin is an epoxy resin.

7. The microlens array of claim 1, wherein said light condensing layer is a layer of photosensitive gelatin.

8. The microlens array of claim 1, wherein said light condensing layer is a layer of radiation curable resin.

9. The microlens array of claim 8, wherein the radiation curable resin is selected from the group consisting of acrylate, methacrylate, urethane acrylate, epoxy acrylate, and polyester acrylate.

10. The microlens array of claim 1, wherein said transparent insulation layer is formed by a low temperature plasma deposition process.

11. The microlens array of claim 10, wherein the low temperature plasma deposition process is performed at temperatures within the range of approximately 200 to 400 degrees Celsius.

12. The microlens array of claim 1, wherein said transparent insulation layer is a layer of silicon oxide.

13. The microlens array of claim 1, wherein said transparent insulation layer is a layer of silicon nitride.

14. The microlens array of claim 1, wherein said transparent insulation layer is a layer of silicon oxynitride.

15. The microlens array of claim 1, wherein the microlenses are circular lenses.

16. The microlens array of claim 1, wherein the microlenses are lenticular lenses.

17. The microlens array of claim 1, wherein the microlenses are ovoid lenses.

18. The microlens array of claim 1, wherein the microlenses are rectangular lenses.

19. The microlens array of claim 1, wherein the microlenses are hexagonal lenses.

20. The microlens array of claim 1, wherein said microlens has a thickness of from about 0.3 μm to about 5.0 μm.

21. The microlens array of claim 1, further comprising a spacer layer under said light condensing layer.

22. The microlens array of claim 21, wherein said spacer layer has a thickness of from about 1 μm to about 20 μm.

23. A microlens array for use in an imaging device comprising:

an array of microlenses, each microlens comprising a refractive layer and a transparent insulation layer.

24. The microlens array of claim 23 wherein the refractive layer is a layer of optical thermoplastic.

25. The microlens array of claim 24 wherein the optical thermoplastic is selected from the group consisting of polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, and polystyrene.

26. The microlens array of claim 23 wherein the refractive layer is a layer of polyimide.

27. The microlens array of claim 23 wherein the refractive layer is a layer of thermoset resin.

28. The microlens array of claim 23 wherein the refractive layer is a layer of photosensitive gelatin.

29. The microlens array of claim 23 wherein the refractive layer is a layer of radiation curable resin.

30. The microlens array of claim 29 wherein the radiation curable resin is selected from the group consisting of acrylate, methacrylate, urethane acrylate, epoxy acrylate, and polyester acrylate.

31. The microlens array of claim 23 wherein the transparent insulation layer is formed by a low temperature plasma deposition process.

32. The microlens array of claim 31wherein the low temperature plasma deposition process is performed at temperatures within the range of approximately 200 to 400 degrees Celsius.

33. The microlens array of claim 23 wherein the transparent insulation layer is a layer of silicon oxide.

34. The microlens array of claim 23 wherein the transparent insulation layer is a layer of silicon nitride.

35. The microlens array of claim 23 wherein the transparent insulation layer is a layer of silicon oxynitride.

36. The microlens array of claim 23 wherein the microlenses are circular lenses.

37. The microlens array of claim 23 wherein the microlenses are lenticular lenses.

38. The microlens array of claim 23 wherein the microlenses are ovoid lenses.

39. The microlens array of claim 23 wherein the microlenses are rectangular lenses.

40. The microlens array of claim 23 wherein the microlenses are hexagonal lenses.

41. The microlens array of claim 23 wherein said microlens has a thickness of from about 0.3 μm to about 5.0 μm.

42. The microlens array of claim 23 further comprising a spacer layer under said light condensing layer.

43. The microlens array of claim 42 wherein said spacer layer has a thickness of from about 1 μm to about 20 μm.

44. A solid-state imager comprising:

an array of pixel sensor cells formed at an upper surface of a substrate;

a protective layer formed over said array; and

an array of microlenses formed on said protective layer, each microlens comprising a transparent insulation layer formed over a refractive layer.

45. The imager of claim 44, wherein the imager is a CMOS imager.

46. The imager of claim 44, wherein the imager is a CCD imager.

47. The imager of claim 44, wherein said array of microlenses is formed so that each pixel of said array of pixel sensor cells has a corresponding microlens formed above it.

48. The imager of claim 44, further comprising a color filter layer formed over said protective layer and under said array of microlenses.

49. The imager of claim 44, wherein the refractive layer is a layer of material selected from the group consisting of optical thermoplastic, polyimide, thermoset resin, photosensitive gelatin, and radiation curable resin.

50. The imager of claim 49, wherein the optical thermoplastic is selected from the group consisting of polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, and polystyrene.

51. The imager of claim 49, wherein the radiation curable resin is selected from the group consisting of acrylate, methacrylate, urethane acrylate, epoxy acrylate, and polyester acrylate.

52. The imager of claim 44, wherein the transparent insulation layer is formed by a low temperature plasma deposition process.

53. The imager of claim 52, wherein the low temperature plasma deposition process is performed at temperatures within the range of approximately 200 to 400 degrees Celsius.

54. The imager of claim 44, wherein the transparent insulation layer is a layer of silicon oxide.

55. The imager of claim 44, wherein the transparent insulation layer is a layer of silicon nitride.

56. The imager of claim 44, wherein the transparent insulation layer is a layer of silicon oxynitride.

57. An imager comprising:

an imaging array having a plurality of pixel sensor cells formed at an upper surface of a substrate and providing output data representing an image;

an array of microlenses formed on the imaging array, wherein each microlens has a transparent insulation layer formed over a refractive layer; and

a processor for receiving and processing data representing the image.

58. The imager of claim 57, wherein said arrays and said processor are formed on a single substrate.

59. The imager of claim 57, wherein said arrays are formed on a first substrate and said processor is formed on a second substrate.

60. A method of forming a microlens array for use in an imaging device, said method comprising the steps of:

providing a substrate having an array of pixel sensor cells formed thereon and a protective layer over the cells;

forming a lens forming layer on at least a portion of the protective layer;

forming microlens array from said lens forming layer; and

forming an insulation layer on said microlens array.

61. The method of claim 60, wherein the substrate further comprises a CMOS pixel array formed thereon.

62. The method of claim 60, wherein the substrate further comprises a CCD pixel array formed thereon.

63. The method of claim 60, wherein said step of forming the lens forming layer comprises a spin-coating process.

64. The method of claim 60, wherein the lens forming layer is a layer of material selected from the group consisting of optical thermoplastic, polyimide, thermoset resin, photosensitive gelatin, and radiation curable resin.

65. The method of claim 64, wherein the optical thermoplastic is selected from the group consisting of polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, and polystyrene.

66. The method of claim 64, wherein the radiation curable resin is selected from the group consisting of acrylate, methacrylate, urethane acrylate, epoxy acrylate, and polyester acrylate.

67. The method of claim 60, wherein the insulation layer is a layer of material selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

68. The method of claim 60, wherein said insulation layer forming step comprises a chemical vapor deposition step.

69. The method of claim 60, wherein said insulation layer forming step comprises a low temperature plasma deposition step.

70. The method of claim 69, wherein the low temperature is a temperature within the range of approximately 200 to 400 degrees Celsius.

71. The method according to claim 60, further comprising forming a spacer layer under said microlens array.

72. The method according to claim 71, wherein said spacer layer has a thickness of from about 1 μm to about 20 μm.

73. A method of forming a microlens array for use in an imaging device, said method comprising the steps of:

forming a lens forming layer on an imaging device;

treating said lens forming layer to form a plurality of microlenses; and

forming a radiation transparent insulation layer on each microlens.

74. The method of claim 73, wherein the lens forming layer is a layer of material selected from the group consisting of optical thermoplastic, polyimide, thermoset resin, photosensitive gelatin, and radiation curable resin.

75. The method of claim 74, wherein the optical thermoplastic is selected from the group consisting of polymethylmethacrylate, polycarbonate, polyolefin, cellulose acetate butyrate, and polystyrene.

76. The method of claim 74, wherein the radiation curable resin is selected from the group consisting of acrylate, methacrylate, urethane acrylate, epoxy acrylate, and polyester acrylate.

77. The method of claim 73, wherein said treating step comprises a baking step.

78. The method of claim 77, wherein said baking step is carried out at a temperature within the range of approximately 100 to 350 degrees Celsius.

79. The method of claim 73, wherein said treating step comprises a radiation exposure step.

80. The method of claim 73, wherein the insulation layer is a layer of silicon oxide.

81. The method of claim 73, wherein the insulation layer is a layer of silicon nitride.

82. The method of claim 73, wherein the insulation layer is a layer of silicon oxynitride.

83. The method of claim 73, wherein said insulation layer forming step comprises a chemical vapor deposition step.

84. The method of claim 73, wherein said insulation layer forming step comprises a plasma deposition step carried out at a temperature within the range of approximately 200 to 400 degrees Celsius.

85. The method according to claim 73, further comprising forming a spacer layer under said lens forming layer before formation of said lens forming layer.

86. The method according to claim 85, wherein said spacer layer has a thickness of from about 1 μm to about 20 μm.

87. A method of forming a microlens array for use in an imaging device, said method comprising the steps of:

forming a lens forming layer on an imaging device;

patterning said lens forming layer to form a plurality of lens forming regions;

treating said plurality of lens forming regions to form a plurality of microlenses; and

forming a transparent insulation layer on the plurality of microlenses.

88. The method of claim 87, wherein the lens forming layer is a layer of material selected from the group consisting of optical thermoplastic, polyimide, thermoset resin, photosensitive gelatin, and radiation curable resin.

89. The method of claim 87, wherein the substrate further comprises a CMOS pixel array formed thereon.

90. The method of claim 87, wherein the substrate further comprises a CCD pixel array formed thereon.

91. The method of claim 87, wherein said treating step comprises a baking step.

92. The method of claim 91, wherein said baking step is carried out at a temperature within the range of approximately 100 to 200 degrees Celsius.

93. The method of claim 87, wherein said treating step comprises a radiation exposure step.

94. The method of claim 87, wherein the insulation layer is a layer of material selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

95. The method of claim 87, wherein said insulation layer forming step comprises a chemical vapor deposition step.

96. The method of claim 87, wherein said insulation layer forming step comprises a plasma deposition step carried out at a temperature within the range of approximately 200 to 400 degrees Celsius.

97. The method according to claim 87, further comprising forming a spacer layer under said lens forming layer before formation of said lens forming layer.

98. The method according to claim 97, wherein said spacer layer has a thickness of from about 1 μm to about 20 μm.

99. A method of forming a microlens array for use in an imaging device, said method comprising the steps of:

forming a lens forming layer on an imaging device, wherein the lens forming layer is a layer of material selected from the group consisting of optical thermoplastic, polyimide, and thermoset resin;

patterning said lens forming layer to form a plurality of lens forming regions;

heat treating said plurality of lens forming regions to form a plurality of microlenses; and

depositing a transparent insulation layer on the plurality of microlenses at a temperature within the range of approximately 200 to 400 degrees Celsius.

ABSTRACT

A microlens array for use in a solid-state imager having an improved fill factor. The microlens array includes a plurality of microlenses, each consisting of two layers: a lower refractive layer, and an upper insulation layer. The refractive layer is formed of transparent material with a suitable refractive index which may be optical thermoplastic, polyimide, thermoset resin, photosensitive gelatin, or radiation curable resin. The insulation layer is formed of transparent insulating material such as silicon oxide, silicon nitride, or silicon oxynitride. Due to the refraction of light through the insulation layer, more light at the pixel edges is captured by each microlens, thereby improving the fill factor of the microlens array. Also disclosed are methods for forming the microlens array.

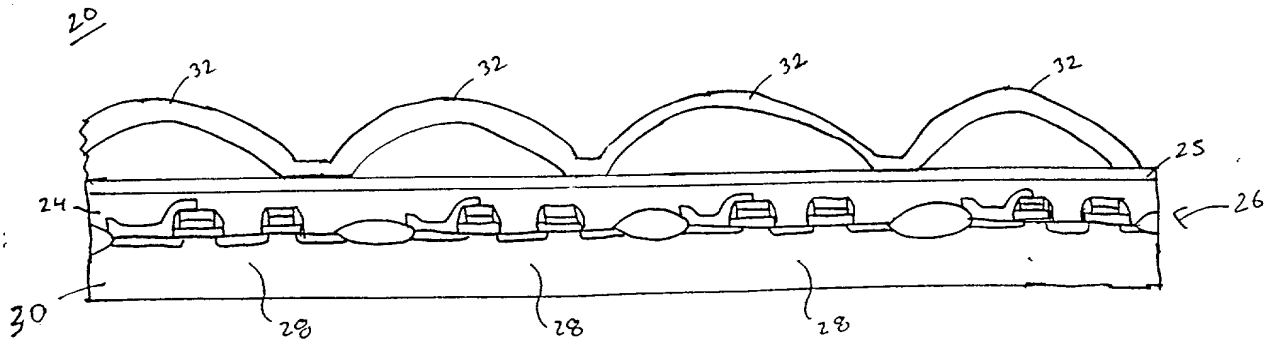

FIG. 1

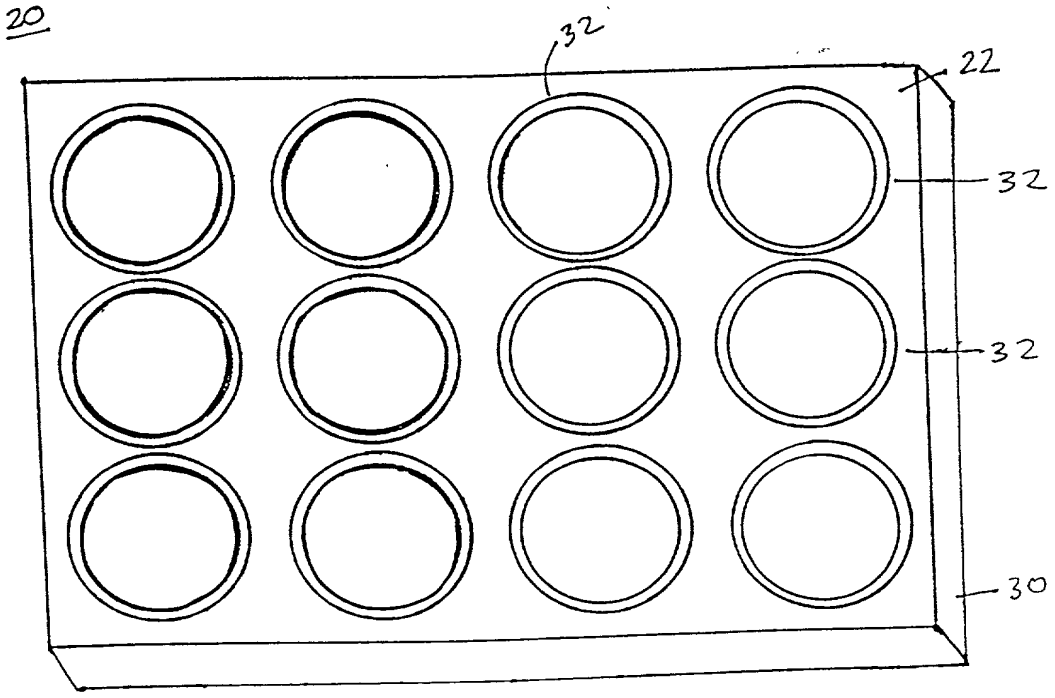

FIG. 2

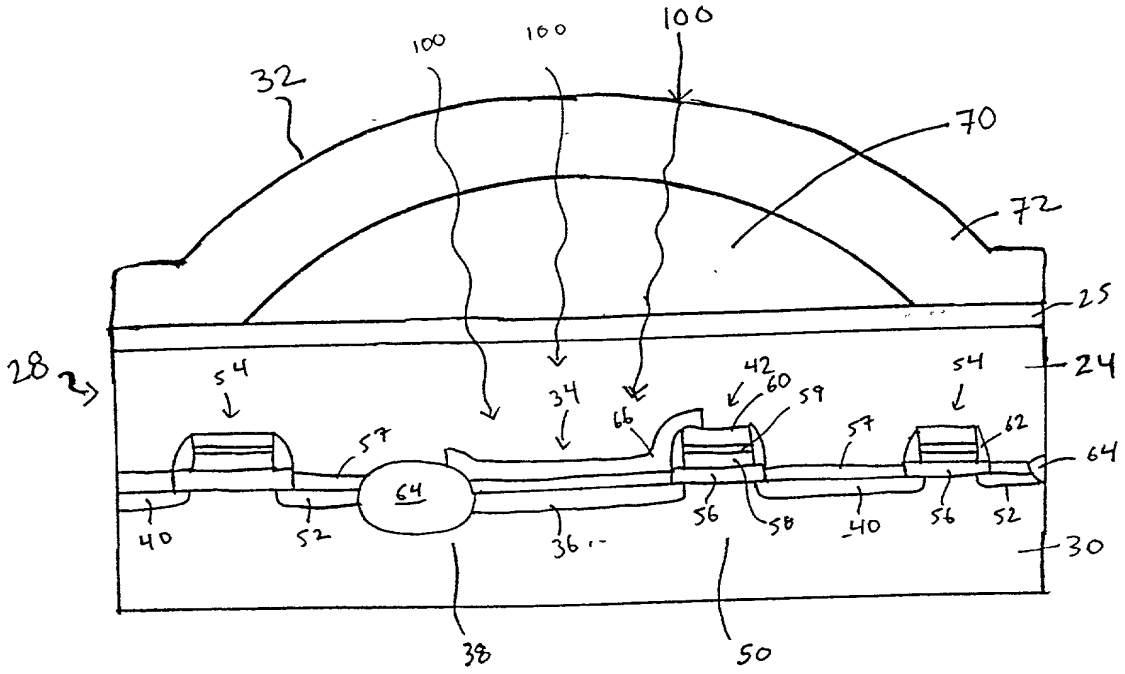
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FIG. 3

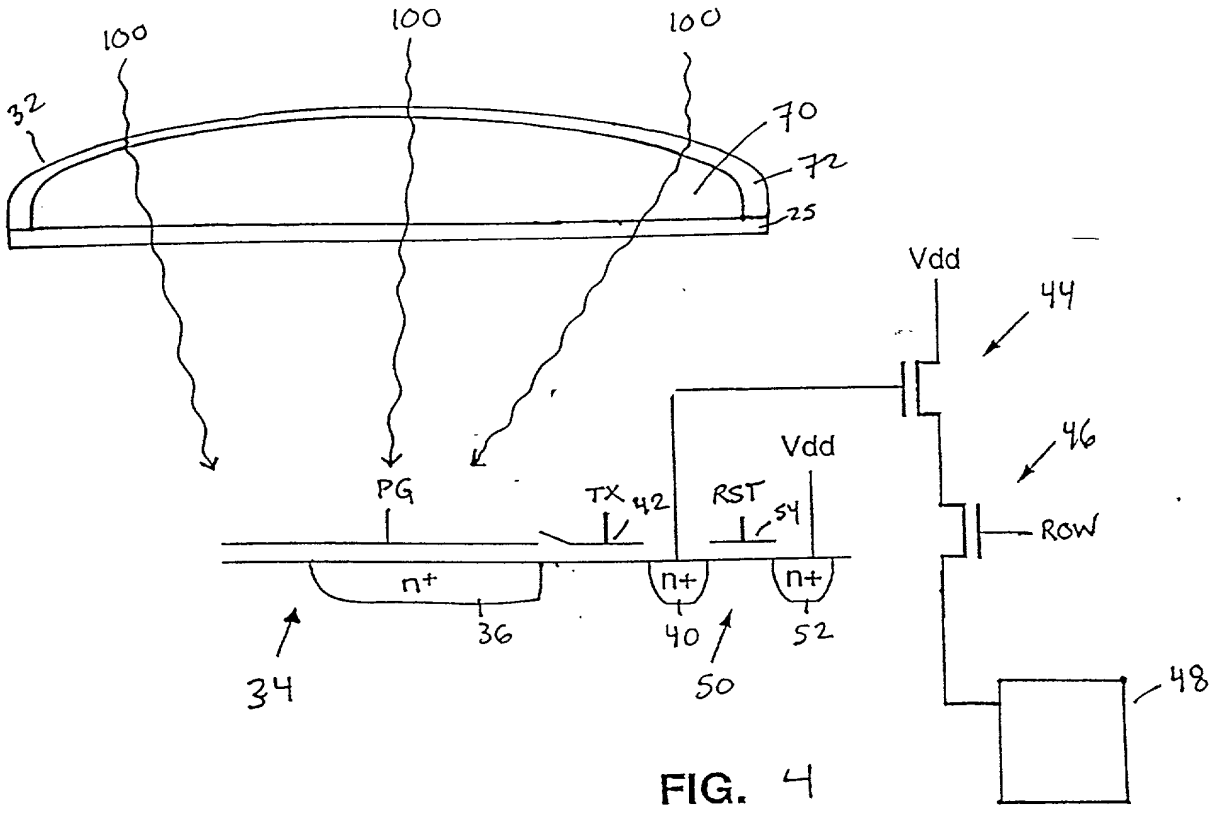
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FIG. 4

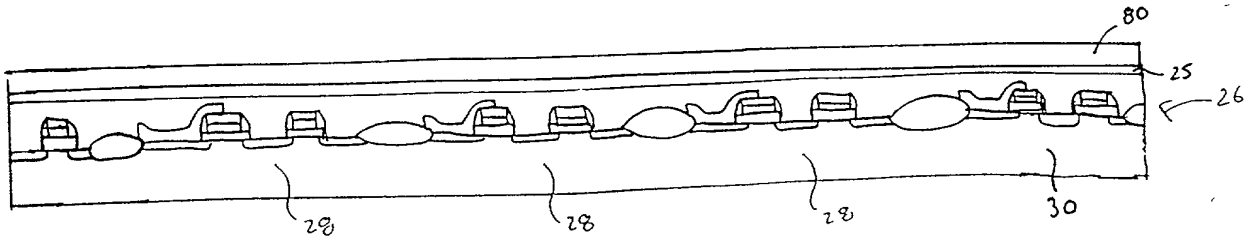

FIG. 5

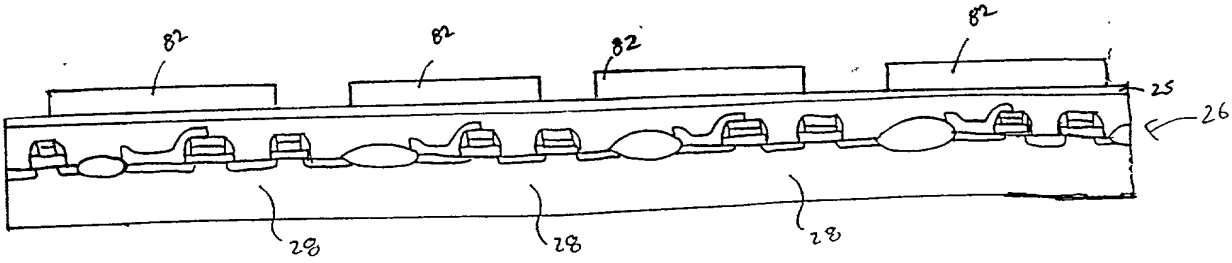

FIG. 6

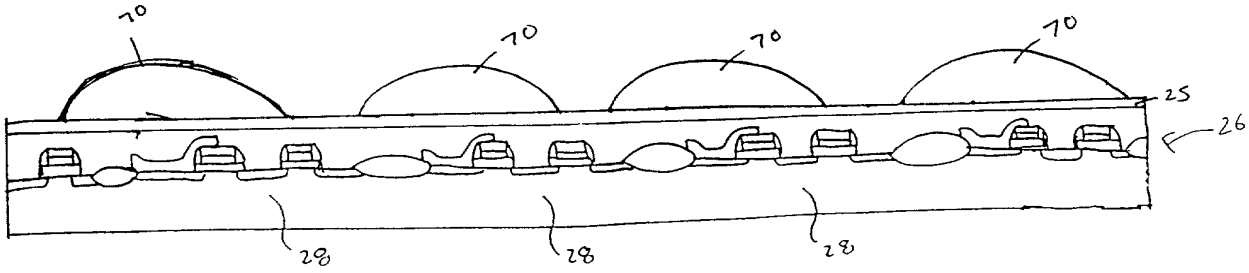

FIG. 7

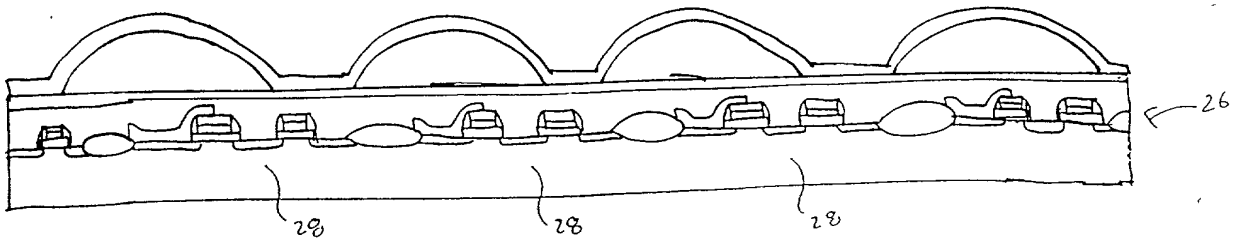
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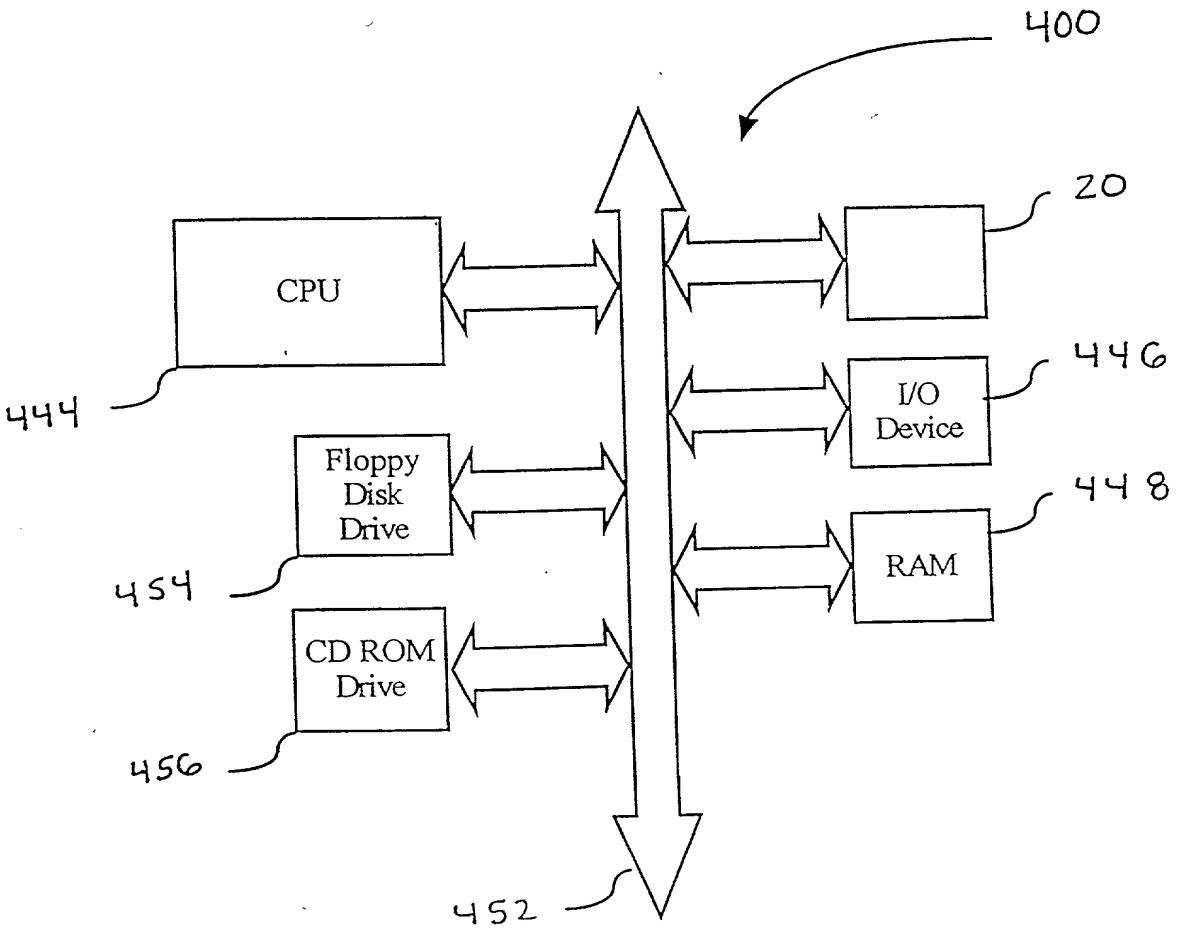
FIG. 8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I/O Device
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Floppy Disk Drive
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RAM
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CD ROM Drive
456
452

Fig. 9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

MICROLENS ARRAY WITH IMPROVED FILL FACTOR

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to **Thomas J. D'Amico** of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526. Telephone calls should be made to Thomas J. D'Amico by dialing (202) 828-2232.

Full name of sole inventor: Howard E. Rhodes

Inventor's signature Howard E Rhodes Date 7/9/99

Residence: Boise, Idaho

Citizenship: United States of America

Post Office Address: 631 E. Ridgefield Drive, Boise, Idaho 83706-9632

PATENT
Docket No.: M4065.0112/P112
Micron No.: 98-0121.00/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application
Inventor: Howard RHODES

Serial No.: Not Yet Assigned Group Art Unit: Not Yet Assigned

Filed: Concurrently Herewith Examiner: Not Yet Assigned

For: MICROLENS ARRAY WITH IMPROVED FILL FACTOR

POWER OF ATTORNEY BY ASSIGNEE AND

CERTIFICATE BY ASSIGNEE UNDER 37 CFR §3.73(b)

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by virtue of the assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526, listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher, 37,131; John R. Fuisz, 37,327; 41,828; Brian A. Lemm, 43,748; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; James M. Silbermann, 40,413; and; and also attorneys Michael L. Lynch, 30,871; Lia M. Pappas, 34,095; W. Eric Webostad, 35,406; and Charles B. Brantley, II, 38,086 of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all

business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Thomas J. D'Amico, Esq.
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, NW
Washington, D.C. 20037-1526
Telephone: (202) 828-2232
Facsimile: (202) 887-0689

MICRON TECHNOLOGY, INC.

Michael L. Lynch
Chief Patent Counsel
Registration No. 30,871

Dated: July 13, 1999